Monolithic 60 GHz GaAs CW IMPATT Oscillators

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Abstract—**A monolithic circuit design was developed for GaAs IMPATT diodes to enable their operation under CW conditions at *V*-band frequencies. All active and passive circuit components were fabricated on the top surface of the GaAs substrate. Good heat dissipation was achieved by distributing the device active area over a large surface area while maintaining a lumped mode of operation. More than 100 mW CW output power was obtained in the 58–65 GHz frequency range, with up to 14.5 percent conversion efficiency. In an alternative design, varactor diodes were integrated with the IMPATT circuits to produce the first monolithic VCO's operating under CW conditions. A tuning bandwidth greater than 3.5 GHz was obtained at a center frequency of 70 GHz, with a maximum CW output power of 40 mW.**

I. Introduction

IMPATT diodes are well known for their high power performance at frequencies extending into the mm-wave range. Many radar systems have a need for high power microwave sources in their transmitters that can only be addressed by the use of IMPATT diodes. At present, all IMPATT diodes are produced in discrete form and operated in external circuits. This technology is a major limitation to the widespread use of IMPATT's in compact, lightweight, low-cost systems that require a higher degree of integration. The application of modern MMIC technology to the fabrication of monolithic IMPATT's has so far been unsuccessful. Alternative methods of fabricating active and passive circuit components on a single chip have been tried in the past [1]–[3]. Although these methods were not directly compatible with mainstream MMIC technology, the results obtained showed promise for improving processing yield and uniformity, lowering unit cost, and enchancing device performance. More recently, monolithic integration of IMPATT oscillators with radiating elements was achieved [4], [5] using MMIC compatible technology.

The prime difficulty in the integration of IMPATT's on the top surface of GaAs is the removal of excess heat. Since IMPATT diodes are particularly high power devices and the GaAs substrate has a notoriously low thermal conductivity (0.46 W/cm °C at 300 K), direct placement of the diodes on the GaAs surface results in an unacceptably high thermal resistance. The second difficulty is the fabrication of impedance matching circuits to extract power efficiently. The impedance levels of millimeter wave IMPATT's under large signal operating conditions are low (typically in the 1–4 Ω range), therefore parasitic circuit elements between the diode and the matching circuits must be minimized.

We have developed design and fabrication techniques that overcome these difficulties. To reduce the thermal resistance, the device was spread over a large surface area using a matrix of small mesas. A self-aligned contact fabrication technique was used to minimize series resistances. All mesas were connected together and to the impedance matching circuitry by the use of air bridges. As a demonstration of this technology, *V*-band CW oscillators and VCO's were fabricated. This paper describes the fabrication techniques and test results obtained with circuits operating in the 55–75 GHz range.

II. Design and Fabrication

All epitaxial layers used in this study were grown by MOCVD on a semi-insulating (SI) GaAs substrate. Si and Zn were used as the n- and p-type dopants. A typical device structure is as shown in Table I. A thick n^+ layer was used as the contact to the n layer. The diode active area was divided into small sections and spread over a larger surface area to provide an effective heat sink. In such a design there are several trade-offs to be made. The total area over which the device is spread must be kept as small as possible to maintain the lumped operation. This is also essential for minimizing the parasitic capacitive elements. To satisfy these conditions, the largest dimension of the heat sink area was kept below $\lambda_g/10$, where λ_g is the wavelength in GaAs. The size of each diode section is chosen by considering the fabrication tolerances and thermal resistance of each section. A large number of possible section sizes and separations between sections was analyzed for optimum performance. A design that produces the maximum CW output power was achieved by maximizing the total device size for a given spread area. The results discussed in this paper were obtained using 5-μm-diameter IMPATT mesas placed on 25-μm centers. A matrix of 2×5 mesas were used for a total device area of 2×10^{-6} cm^2.

Major fabrication steps involved in the realization of monolithic IMPATT circuits are shown in Fig. 1. A brief description of these steps is given below. As a first step, individual IMPATT sections were defined by TiPtAu evaporation and lift-off (Fig. 1(a)). These sections were then mesa-isolated by the use of BCl_3 reactive ion etching (Fig. 1(b)). This type of isolation produces less than 100-nm undercuts so that the device area is precisely defined.

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TABLE I
THE IMPATT STRUCTURE

LAYER	Doping (cm^{-3})	Thickness (μm)
p^+	5×10^{18}	0.30
p	2×10^{17}	0.25
n	1.6×10^{17}	0.30
n^+	3×10^{18}	1.00
Substrate	Undoped	500

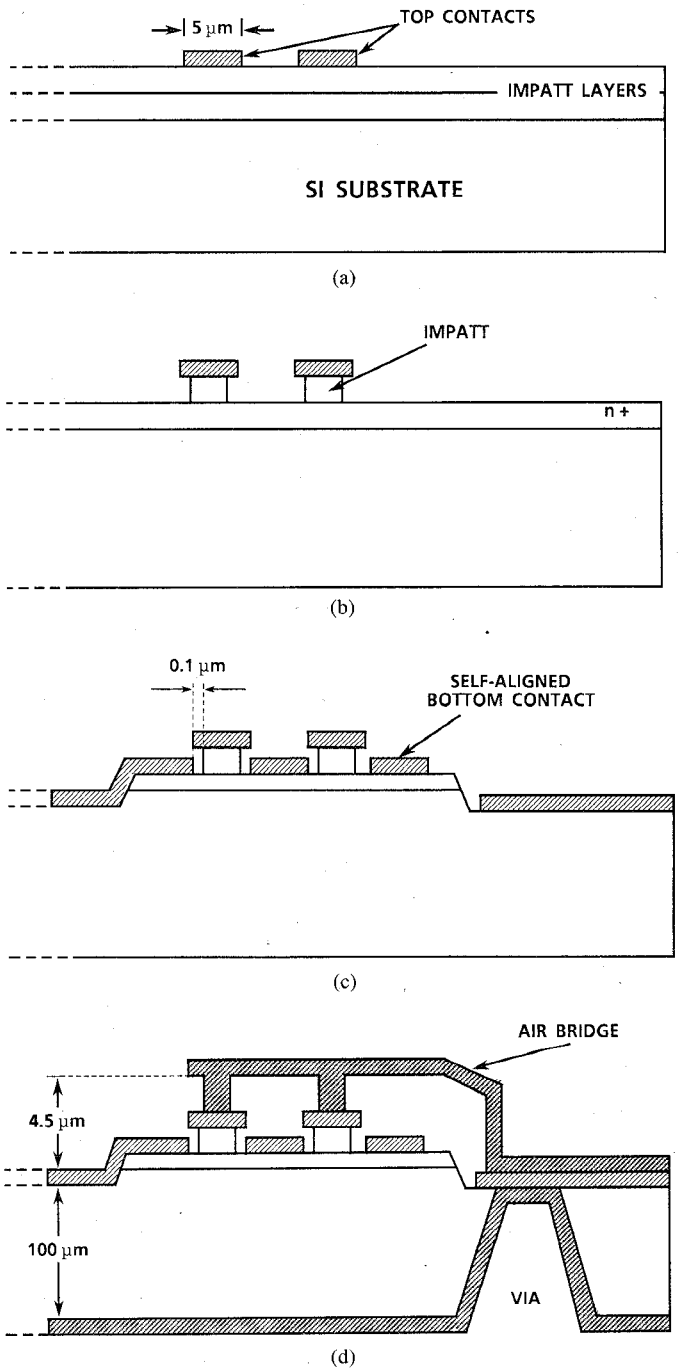


Fig. 1. Major fabrication steps involved in the realization of monolithic IMPATT circuits

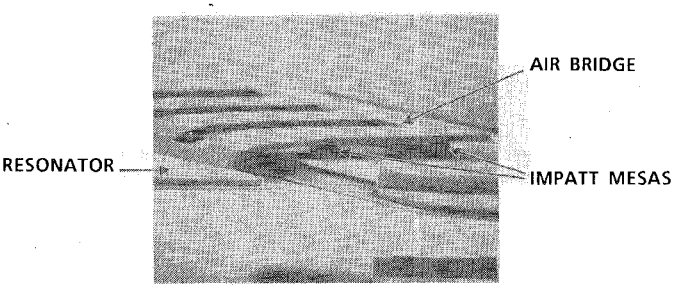


Fig. 2. SEM picture of the air-bridge connections to IMPATT mesas.

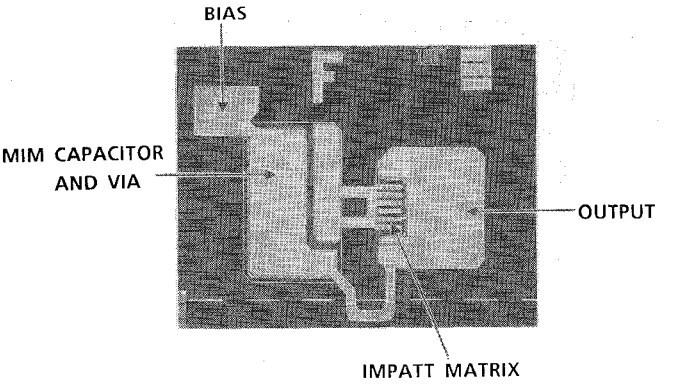


Fig. 3. SEM picture of the monolithic IMPATT oscillator.

Since the device area is divided into many segments, the total device edge/area ratio is proportionally increased. It is therefore important that the mesa edges are passivated to reduce surface leakage currents. A 200-nm-thick, plasma-enhanced-deposition Si_3N_4 film was used for this purpose. Another mesa isolation was used to separate n^+ layers. A self-aligned technique was then used to produce contacts to the n^+ layer [6] (Fig. 1(c)). Passive circuit elements such as transmission lines, MIM capacitors, and inductors were produced on the surface of the SI GaAs substrate. A 4.5-μm tall air bridge was used to connect individual IMPATT mesas to the impedance matching circuitry (Fig. 1(d)). A close-up of the air bridge connection is shown in Fig. 2. Via holes were used to ground one terminal of the device. Fig. 3 shows the completed 60 GHz oscillator circuit. As seen in this figure, the diode impedance was matched to the line impedance of 50 Ω by the use of short sections of the high impedance transmission line in series with quarter-wave impedance transformers. A bias filter was provided by the use of a large MIM capacitor and a quarter-wave high impedance transmission line. Typical dc yields from 2-in wafers were 80 percent.

III. Results and Discussion

A. Thermal Considerations

Since the thermal conductivity of GaAs is approximately one-tenth that of silver, the performance of monolithic IMPATT circuits depends strongly on the thermal designs employed. In the absence of thermal limitations, we can expect the output power from an IM-

TABLE II
SURFACE TEMPERATURE RISE FOR A 2 × 5 MATRIX

Mesa Diameter (μm)	Mesa Spacing (μm)	Maximum Surface Temperature Rise ($°C$)
5	15	442
	25	330
	50	276
10	15	8293
	25	4573
	50	2706

PATT diode to increase linearly with the diode's area. This is typically the case when IMPATT diodes are operated adjacent to diamond heat sinks. This is also the case when the device is operated under very short (<200 ns) pulses. The size of a single IMPATT mesa in monolithic circuits is, however, severely limited if CW operation is needed. As it will be shown in the analysis below, the mesa diameters must be kept below 10 μm. Any increase in output power therefore must come from the use of multiple mesas arranged in such a way that thermal coupling among them is minimized. Also the total area over which the mesas matrix is spread must not exceed the $\lambda_g/10$ restrictions mentioned above. To illustrate the effect of the size and separation among the mesas, the surface temperature rise was calculated for a 2 × 5 mesa matrix using the method of Linsted and Surty [7]. In these calculations, the dissipated power density was kept constant at 5×10^5 W/cm^2. The results are shown in Table II. As expected, the temperature rise decreases as the mesa size is reduced and also as the mesas are separated further from one another. Among the conditions considered here, the lowest thermal resistance is obtained with 5-μm-diameter mesas placed 50 μm from one another. As mesas are moved closer to one another, for example, from 50 μm to 15 μm, the thermal resistance increases by a factor of 1.6 for 5-μm mesas and a factor of 3 for 10-μm mesas. The other significant result seen in Table II is that a matrix of 10-μm-diameter mesas produces 10 to 20 times higher surface temperatures than their 5-μm counterparts separated by the same distances. It is obvious that the size of individual mesas is more significant in the thermal design than the separation between them. A more detailed analysis of 5-μm-diameter mesas separated by 25 μm is given below.

Fig. 4 shows the calculated temperature rise as a function of distance on the surface and within the GaAs substrate. The heat was assumed to be generated on the top surface of the wafer for these calculations. It was further assumed that heat was dissipated solely through the GaAs substrate by conduction, i.e., heat dissipation by radiation and heat conduction through the topside metallization were not included. It is seen in this figure that the temperature rise on the surface of the substrate is sharply localized. This is due basically to the poor thermal conductivity of GaAs. The minimization of the mesa size is

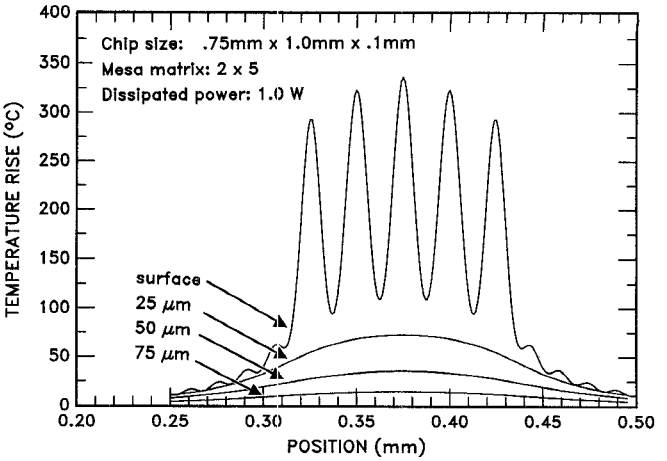


Fig. 4. The theoretical steady-state temperature rise across the IMPATT mesas as a function of position for a 2 × 5 mesa matrix and 5-μm-diameter mesas. The depth position is with reference to the substrate top surface.

therefore essential to lower the peak temperature. The distance between mesas adjusts the thermal coupling between them. In the design discussed here, the temperatures between mesas drop down to less than 30 percent of their peak values. Further separation can increase the maximum/minimum temperature ratio, but this is accomplished at the expense of increased electrical parasitics. Fig. 4 shows that for a dissipated power of 1.0 W, the maximum temperature is 330°C at the center of the mesa matrix. This indicates that the maximum thermal resistance of the chip (not including the chip carrier) is 330°C/W for this design. Also seen in Fig. 4 is the nonuniform heat distribution across the mesa matrix. The temperature has a maximum at the center and gradually decreases toward the edges. In actual devices this effect may not be as pronounced, however, due to the temperature dependent breakdown voltage of p–n junctions. The device thermal resistance is probably better estimated as the average of the temperature peaks. The total measured thermal resistance of the monolithic chip soldered to a copper carrier was 355°C. This value is in general agreement with the calculated chip thermal resistance and further points out that most of the thermal resistance is due to the chip itself. A thermal resistance reduction of approximately 50°C/W can be achieved by the use of 0.05-mm-thick substrates rather than the 0.1-mm-thick one used here.

B. Millimeter-wave Oscillators

The mm-wave testing was carried out in a *V*-band waveguide test setup. A fineline microstrip-to-waveguide transition was used to couple the power from the monolithic chip to the waveguide. A typical variation of ∓ 1 GHz was found in the free-running oscillation frequency of monolithic oscillators from a 2-in wafer. Most devices were operated without the need for external tuning. The best results were obtained from flat-profile double-drift IMPATT structures such as the one shown in Table I. The

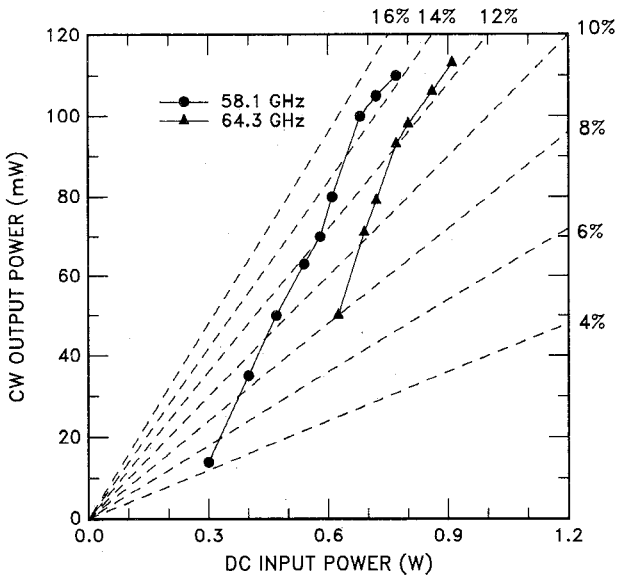


Fig. 5. The oscillator output characteristics for two different monolithic circuits on the same wafer.

output characteristics of two circuits operating in mid-V-band frequencies are shown in Fig. 5. At 58.1 GHz, 110 mW CW output power was obtained with 14.5 percent conversion efficiency. This is the highest efficiency reported for GaAs IMPATT's at this frequency. A CW output power of 100 mW and a conversion efficiency of 12.5 percent were obtained with the second design (on the same wafer) at 64.3 GHz with an estimated junction temperature of 265°C. At an elevated junction temperature of 305°C, the output power was 115 mW with 12.7 percent efficiency. It is seen in this figure that the output powers from both circuits are still increasing at the highest dc bias point, whereas the device efficiencies are saturated. This indicates that the monolithic devices are operating under thermally limited conditions but the RF voltage swings are close to their optimum values. No drastic increase in output power is therefore expected under pulsed bias conditions for this design.

In an alternative design, monolithic VCO circuits were fabricated. This circuit included an oscillator circuit similar to the one described above and a varactor circuit on the same chip. The varactor diodes were fabricated by removing the p-type portion of the IMPATT structure and producing Schottky contacts to the n-type drift layer. The fabrication of the varactor diodes was similar to the fabrication of IMPATT's. In this design two 5-μm-diameter varactors and a 2 × 4 matrix of IMPATT mesas were employed for a total IMPATT area of 1.6×10^{-6} cm^2. The varactor was biased with respect to the IMPATT diodes through a low-pass biasing circuit. Fig. 6 shows an equivalent circuit of the VCO. In this figure, C_d, C_a, and C_v are the capacitances of the IMPATT diode, the parasitic capacitance due to the air bridge, and the varactor diode capacitance respectively. Typically, the C_a/C_d ratio is 0.15. C_1 and C_2 are MIM capacitors with values of 20 and 11 pF, respectively. Fig. 7 is a SEM

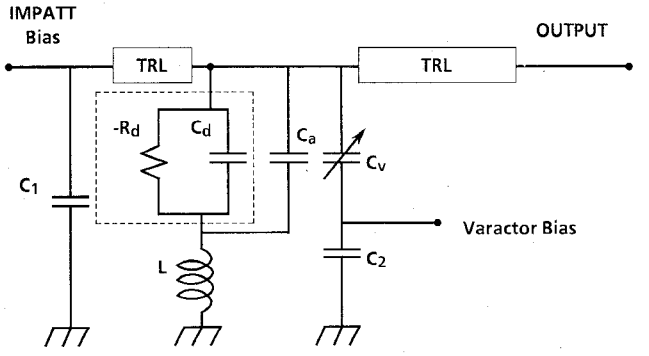
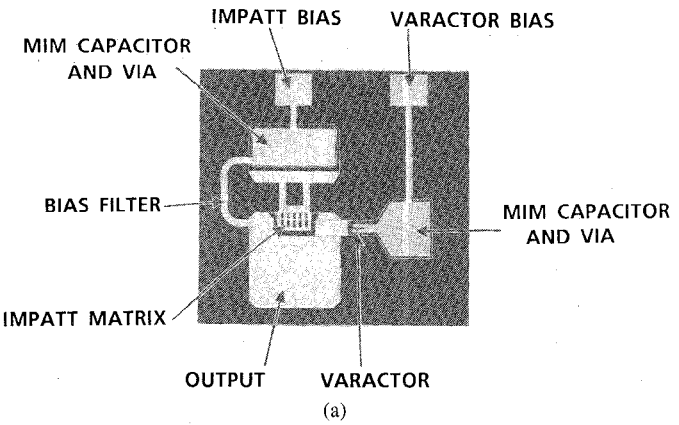
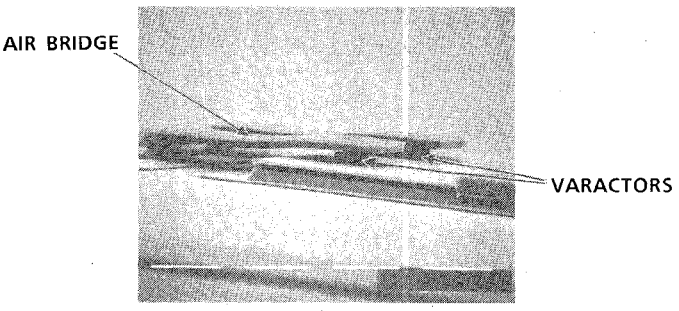


Fig. 6. The equivalent circuit of the monolithic IMPATT VCO.



(a)



(b)

Fig. 7. (a) SEM picture of the monolithic IMPATT VCO. (b) SEM picture of the air-bridge connections to varactors.

picture of the completed circuit and a close-up of the air-bridge connections to the varactors. The tuning behavior is shown in Fig. 8. A tuning range of more than 3.5 GHz was achieved at a center frequency of 70 GHz. The VCO circuit produced a CW output power of 40 mW at 72.2 GHz, with an estimated junction temperature of 175°C. This result, to the best of our knowledge, represents the first monolithic CW IMPATT VCO.

IV. Conclusions

Monolithic design and fabrication techniques were developed for GaAs IMPATT diodes. These techniques are entirely compatible with standard MMIC technology. As a demonstration, V-band CW oscillators and VCO's were fabricated and tested. The monolithic circuits produced

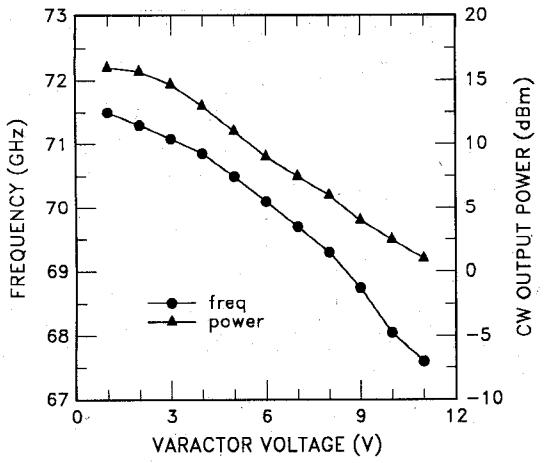


Fig. 8. Tuning characteristics of the monolithic VCO.

state-of-the-art efficiencies, tuning bandwidths, and yields.

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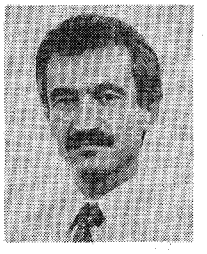

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